CLAIMS

What is claimed is:

1. A method of prefetching data from a memory (450) to a cache (460), comprising: determining (326) a first measure of equal-stride memory accesses, based on a plurality of equal-stride memory accesses and a prior stride value (412), determining (322) a second measure of non-equal-stride memory accesses, based on a plurality of non-equal-stride memory accesses and the prior stride value (412), effecting (130) a prefetch of the data from the memory (450) based on the first measure, and effecting (230) a modification of the prior stride value (412) based on the second measure.

2. The method of claim 1, wherein determining the first measure and the second measure is effected by maintaining a count (414) that is incremented (326) for each equal-stride memory access and decremented (322) for each non-equal-stride memory access, and effecting the prefetch and effecting the modification are each based (330) on the count (414).

3. The method of claim 2, wherein effecting (130) the prefetch occurs when (330) the count (414) is equal or above an upper limit, and effecting (230) the modification occurs when (330) the count (414) is equal or below a lower limit.

4. The method of claim 3, wherein the count (414) is limited to a maximum of three, the upper limit is two, and the lower limit is one.

5. A prefetch system (400) comprising: a control register (410) that is configured to contain at least one measure (414) that corresponds to a consistency of stride values between requested memory accesses, a prefetch controller (430) that is configured to prefetch data from a memory (450) to a cache (460), based on the measure of consistency, wherein the consistency of stride values is dependent upon a comparison of a current stride with a prior stride value (412), the prefetch controller (430) is further configured to modify the prior stride value (412) based on a measure of inconsistency, and the measure of inconsistency is based on a plurality of non-equal-strides between requested memory accesses.

6. The prefetch system (400) of claim 5, wherein the measure of consistency and the measure of inconsistency correspond to a count (414) that is incremented upon each equal-stride requested memory access, up to a maximum count, and decremented upon each non-equal-stride requested memory access, down to a minimum count.

7. The prefetch system (400) of claim 6, wherein the prefetch controller (430) is configured to: prefetch the data when the count (414) is equal or above an upper threshold level, and modify the prior stride value (412) when the count (414) is equal or below a lower threshold level.

8. The prefetch system (400) of claim 7, wherein the maximum count is three, the upper threshold level is two, the lower threshold level is one, and the minimum count is zero.

9. A processing system, comprising: a memory (450) that is configured to provide access to data based on an access address, a cache (460), operably coupled to the memory (450), that is configured to store data that is accessed from the memory (450), to facilitate rapid access to the data, a processor (420), operably coupled to the memory (450) and the cache (460), that is configured to provide the access address and to receive the data from the cache (460), if it is stored in the cache (460), or from the memory (450), if it is not stored in the cache (460), and a fetch controller (430), operably coupled to the processor (420), the memory (450), and the cache (460), that is configured to effect a transfer of data from the memory (450) to the cache (460), based on the access address and a predicted stride value, wherein the fetch controller (430) is further configured to maintain a measure of stride consistency that is based on repeat occurrences of equal stride values, and a measure of stride inconsistency that is based on repeat occurrences of unequal stride values, and he fetch controller (430) effects the transfer of data based on the measure of stride consistency, and effects a modification of the predicted stride value based on the measure of stride inconsistency.

10. The processing system of claim 9, wherein the measure of stride consistency and the measure of stride inconsistency are each based on a count (414) that is incremented upon each equal-stride requested memory access, up to a maximum count, and decremented upon each non-equal-stride requested memory access, to a minimum count.

11. The processing system of claim 10, wherein the fetch controller (430) is configured to: effect the transfer of data when the count (414) is equal or above an upper threshold level, and effect the modification of the predicted stride value when the count (414) is equal or below a lower threshold level.

12. The processing system of claim 11, wherein the maximum count is three, the upper threshold level is two, the lower threshold level is one, and the minimum count is zero.